Bonus Question

Two 16-bit 2-to-1 mux is needed. Netlist 11 shows a 16-bit 2-to-1 mux. It consists of 16 instances of the 1-bit 2-to-1 mux, with the select bit the same across each instance.

```
subckt MUX2_16 VDD VSS\
A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0\
B15 B14 B13 B12 B11 B10 B9 B8 B7 B6 B5 B4 B3 B2 B1 B0\
s\
o15 o14 o13 o12 o11 o10 o9 o8 o7 o6 o5 o4 o3 o2 o1 o0
parameters size=1
M15 (VDD VSS A15 B15 s o15) MUX15 size=size
M14 (VDD VSS A14 B14 s o14) MUX14 size=size
M13 (VDD VSS A13 B13 s o13) MUX13 size=size
M12 (VDD VSS A12 B12 s o12) MUX12 size=size
M11 (VDD VSS A11 B11 s o11) MUX11 size=size
M10 (VDD VSS A10 B10 s o10) MUX10 size=size
M9 (VDD VSS A9 B9 s o9) MUX9 size=size
M8 (VDD VSS A8 B8 s o8) MUX8 size=size
M7 (VDD VSS A7 B7 s o7) MUX7 size=size
M6 (VDD VSS A6 B6 s o6) MUX6 size=size
M5 (VDD VSS A5 B5 s o5) MUX5 size=size
M4 (VDD VSS A4 B4 s o4) MUX4 size=size
M3 (VDD VSS A3 B3 s o3) MUX3 size=size
M2 (VDD VSS A2 B2 s o2) MUX2 size=size
M1 (VDD VSS A1 B1 s o1) MUX1 size=size
M0 (VDD VSS A0 B0 s o0) MUX0 size=size
ends MUX2_16
```

Netlist 11 16-bit 2-to-1 MUX

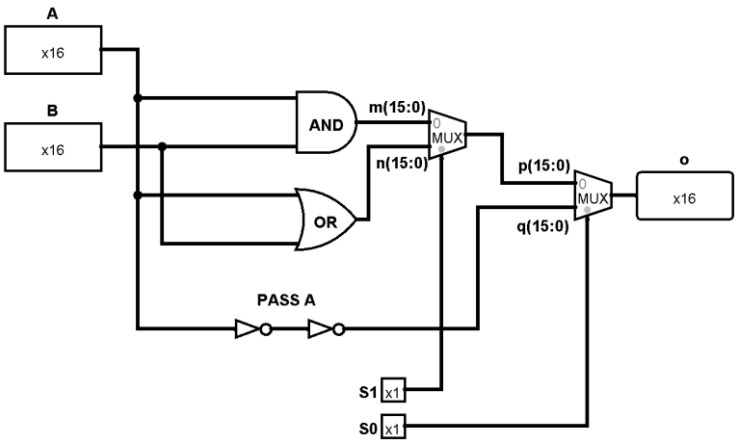

Figure 10 Block Diagram of the mux select structure

Figure 10 shows a block diagram of the select structure. Wires names (signal names) are labelled on the diagram, and they corresponds to the ones specified in the netlist below. Netlist 12 impalements the desired structure. The first mux select from the result of the AND and OR gate and the second mux select for the PASS gate.

```
subckt Comp VDD VSS\
A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0\
B15 B14 B13 B12 B11 B10 B9 B8 B7 B6 B5 B4 B3 B2 B1 B0\
s1 s0\
o15 o14 o13 o12 o11 o10 o9 o8 o7 o6 o5 o4 o3 o2 o1 o0
parameters size=1

and (A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0\
B15 B14 B13 B12 B11 B10 B9 B8 B7 B6 B5 B4 B3 B2 B1 B0\
n15 n14 n13 n12 n11 n10 n9 n8 n7 n6 n5 n4 n3 n2 n1 n0) AND2_16

or (A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0\
B15 B14 B13 B12 B11 B10 B9 B8 B7 B6 B5 B4 B3 B2 B1 B0\
m15 m14 m13 m12 m11 m10 m9 m8 m7 m6 m5 m4 m3 m2 m1 m0) OR2_16

M1 (VDD VSS\
n15 n14 n13 n12 n11 n10 n9 n8 n7 n6 n5 n4 n3 n2 n1 n0\
m15 m14 m13 m12 m11 m10 m9 m8 m7 m6 m5 m4 m3 m2 m1 m0\
s1\
p15 p14 p13 p12 p11 p10 p9 p8 p7 p6 p5 p4 p3 p2 p1 p0) MUX2_16

pass (vdd! 0\
A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0\
q15 q14 q13 q12 q11 q10 q9 q8 q7 q6 q5 q4 q3 q2 q1 q0) PASS_16

M0 (VDD VSS\
p15 p14 p13 p12 p11 p10 p9 p8 p7 p6 p5 p4 p3 p2 p1 p0\
q15 q14 q13 q12 q11 q10 q9 q8 q7 q6 q5 q4 q3 q2 q1 q0
s0\
o15 o14 o13 o12 o11 o10 o9 o8 o7 o6 o5 o4 o3 o2 o1 o0) MUX2_16

ends Comp
```

Netlist 12 The selection circuit